What is claimed is:

[Claim 1] 1. A method of manufacturing a non-volatile memory cell, comprising:

forming a first dielectric layer over a substrate;
forming a second dielectric layer having a trench over the first dielectric layer;
forming a pair of charge storage spacers on sidewalls of the trench;
forming a third dielectric layer over the substrate to cover the first dielectric layer, the charge storage spacers and the second dielectric layer;
forming a conductive structure on a position over the charge storage spacers on the third dielectric layer;
removing portions of the third dielectric layer, the second dielectric layer and first dielectric layer not covered by the conductive structure; and
forming source/drain regions in the substrate at each side of the conductive structure.

[Claim 2] 2. The method of claim 1, wherein the first dielectric layer comprises a silicon oxide layer.

[Claim 3] 3. The method of claim 1, wherein forming the pair of charge storage spacers on the sidewalls of the trench comprises:

forming a charge storage material layer over the substrate; and
etching back the charge storage material layer.

[Claim 4] 4. The method of claim 3, wherein an etching selectivity of the charge storage material layer has different etching selectivity from the second dielectric layer.

[Claim 5] 5. The method of claim 4, wherein the charge storage material layer is a silicon nitride layer or a silicon oxynitride layer.

[Claim 6] 6. The method of claim 3, wherein the charge storage material layer comprises a doped polysilicon layer.

[Claim 7] 7. The method of claim 6, further comprising a step of performing an annealing process after etching back the charge storage material layer so as to eliminate damage of the charge storage material layer caused by the etching-back process.

[Claim 8] 8. The method of claim 6, wherein the third dielectric layer is a silicon oxide-silicon nitride-silicon oxide layer or a silicon oxide-silicon nitride layer or a silicon oxide layer.

[Claim 9] 9. The method of claim 1, further comprising a step of forming a pair of dielectric spacers on sidewalls of the conductive structure before removing portions of the third dielectric layer, the second dielectric layer and first dielectric layer not covered by the conductive structure.

[Claim 10] 10. A method of manufacturing a flash memory cell, comprising:

forming a tunneling dielectric layer over a substrate;
forming a patterned dielectric layer having a trench over the tunneling dielectric layer;
forming a conductive layer over the substrate to cover a surface of the trench;
removing portions of the conductive layer to form a pair of conductive spacers on sidewalls of the trench;
forming an inter-gate dielectric layer over the substrate to cover the patterned dielectric layer, the pair of the conductive spacers and the tunneling dielectric layer;

forming a control gate on a position corresponding to the conductive spacers on the inter-gate dielectric layer; and
forming source/drain regions in the substrate at each side of the control gate.

[Claim 11] 11. The method of claim 10, wherein the tunneling dielectric layer comprises a silicon oxide layer.

[Claim 12] 12. The method of claim 10, further comprising a step of performing an annealing process after removing portions of the conductive layer.

[Claim 13] 13. The method of claim 10, wherein the inter-gate dielectric layer is a silicon oxide-silicon nitride-silicon oxide layer or a silicon oxide-silicon nitride layer or a silicon oxide layer.

[Claim 14] 14. The method of claim 10, wherein after forming the control gate, the method further comprising:

forming a pair of dielectric spacers on sidewalls of the control gate, wherein a portion of the inter-gate dielectric layer is exposed; and
removing the exposed inter-gate dielectric layer, the patterned dielectric layer and the tunneling dielectric layer.

[Claim 15] 15. A method of manufacturing a silicon-oxide-nitride-oxide-silicon (SONOS) memory cell, comprising:

forming a pad oxide layer over a substrate;
forming a patterned dielectric layer having a trench over the pad oxide layer;
forming a charge-trapping layer over the substrate to cover the trench;
removing portions of the charge-trapping layer to form a pair of charge-trapping spacers on sidewalls of the trench;

forming a top oxide layer over the substrate to cover the surface of the patterned dielectric layer, the pair of the charge-trapping spacers and the pad oxide layer;
forming a gate on the top oxide layer over the charge-trapping spacers; and
forming a source/drain region in the substrate at each side of the gate.

[Claim 16] 16. The method of claim 15, wherein an etching selectivity of the patterned dielectric layer is different from an etching selectivity of the charge-trapping layer.

[Claim 17] 17. The method of claim 15, wherein the charge-trapping layer is a silicon nitride layer or a silicon oxynitride layer.

[Claim 18] 18. The method of claim 15, wherein after forming the gate, the method further comprising:

forming a pair of dielectric spacers on sidewalls of the gate, wherein a portion of the top oxide layer is exposed; and
removing the exposed top oxide layer, the patterned dielectric layer and the pad oxide layer underneath.